PROJECT DESCRIPTION

Title: *A Micro Thermoelectric Cryogenic Cooler for MEMS*

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Work Began: 03/01/2006
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Funding Source: DARPA

Project Goals:

A micro cryogenic cooler based on thermoelectric effects could have a major impact on critical military, medical, and consumer applications including substantial performance improvement of existing systems such as infrared detectors for military applications and localized quenching of biological tissues. Additionally, resonant MEMS, such as filters and gyroscopes benefit from an increase in quality factor at reduced temperatures. Because it has a lower efficiency than traditional cooling techniques, thermoelectric cooling has not been widely exploited for macro-scale cooling. However, for micro/nanoscale applications, efficiency may not be the most important technical consideration; rather size, total power consumption, and simplicity of fabrication and operation become critical issues. Because a thermoelectric micro cooler requires no moving parts or fluidic connections it could provide a robust solution for cooling a large variety of MEMS and IC-based microsystems. The ultimate goal of this project is developing a multistage micro thermoelectric cryogenic cooler capable of achieving a temperature of 160K, heat lift of up to a maximum of 5mW within a volume of less than 0.2cc, and using less than 100mW of power.

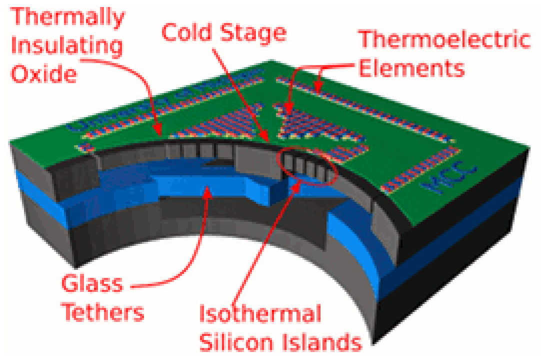

Figure 1: A schematic view of TE cooler.

Approach and Methodology:

To achieve the project goal, research and development is necessary in: 1) isolation techniques to reduce thermal loss, 2) multistage TE cooler optimization to maximize temperature differentials, 3) low-temperature die attachment and vacuum packaging techniques, 4) reliable production of high-performance TE materials. Figure 1 illustrates the overall structure of the “Cool MEMS” TE cooler. The thermoelectric materials are deposited on top of a thermally isolating structure made from silicon and silicon dioxide. This structure is suspended in a silicon frame and supported from below by a glass tether to provide some additional mechanical support. A fully completed device would also include cap for vacuum packaging and a MEMS or IC chip mounted in the center of the cooler. Signals would be transferred out using sealed feedthroughs.

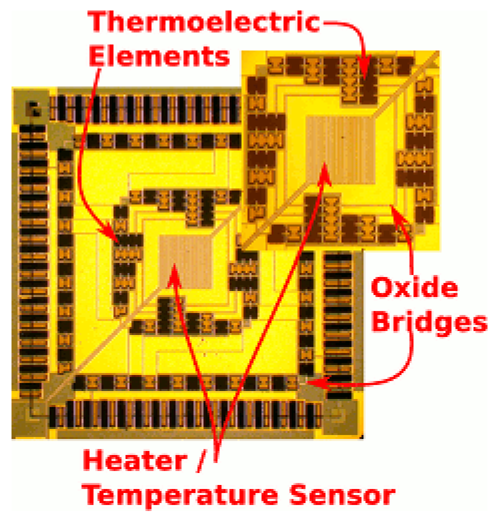

Figure 2: A fabricated 6-stage cooler.

Role in Supporting the Strategic Plan and Testbeds:

This project develops a micro cooler, as well as a low-temperature die attachment and vacuum packaging. This technology could be applied to any MEMS devices that exhibit increased performance when operated at temperatures below ambient. This project supports the Environmental Monitoring Testbed, through potential applications to various aspects of the GC project, including thermal cycling of the pre-concentrator and cooling the gas sensors used at the output of the separation columns.

Results and Accomplishments:

Work has progressed on the development of a second-generation cooler using the previously developed thermal-isolation platform. The thermal-isolation platform has been designed, fabricated, and tested to serve as the main body of the TE cooler.

The upper layer consists of a series of concentric silicon rings separated by thin oxide bridges, as shown in Figure 2. This structure is supported from below by glass, providing mechanical stability without sacrificing thermal isolation. The microcooler is then implemented on top of this platform by co-evaporating both Bi2Te3 and Sb2Te3 in controlled environments. The co-evaporation has been previously optimized to produce thin films with a thermoelectric figure of merit, ZT, between 0.3 and 0.4, which are among the highest qualities reported so far for thin films of these materials. The resulting cooler has achieved temperature differentials of over 22.3K, as shown in Figure 3, with a power consumption of less than 30mW.

Relevance to Other Work:

Micro TE coolers for integrated electronics have been developed by many groups, but little has been done to explore multistage coolers with planar implementation temperatures. Additionally, this research will result in further development of low-temperature wafer level die attachment and vacuum packaging techniques.

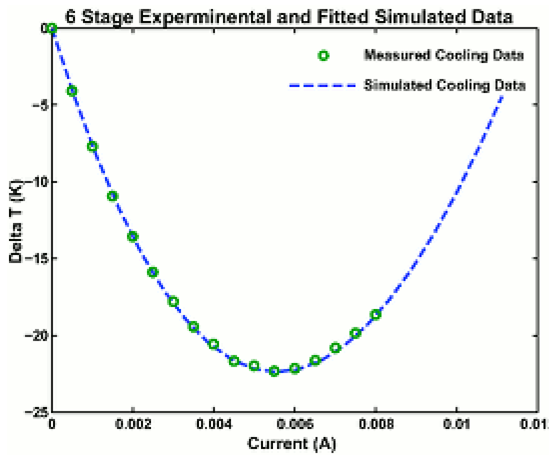

Figure 3: Cooling and power consumption of a 6-stage cooler showing 22.3K cooling.

Plans for the Coming Year:

The primary goals for the coming year are to improve cooler performance, and to integrate the device with die attachment techniques and vacuum packaging technologies. To improve performance, a new fabrication process is being developed that is predicted to achieve differentials of more than 30K by significantly reducing the parasitic thermal effects associated with the current structure. To achieve die attachment and vacuum packaging, techniques currently under development at the University of Michigan will be investigated. Additional plans for the coming year include work to replace the thin-film thermoelectric elements with self-assembled bulk materials.

Expected Milestones and Dates:

- Complete second round of isolation and cooler structure fabrication *(Completed)*
- Complete 3rd-generation cooler based on new fabrication technique (10/15/2009)
- Demonstrate die attachment to cooler (11/20/2009)

Expected Contributions, Deliverables, and Company Benefits:

- Develop low-power, micro thermoelectric cooler for MEMS or IC-based microsystems
- Develop low-temperature, wafer-level, vacuum package
- Develop system integration and assembly techniques

References and Recent Publications:

1. A. Gross et al, “High-Performance Micro Scale Thermoelectric Cooler: An Optimized 6-Stage Cooler,” Presented at *Transducers 2009,* pp. 2413–2416.
2. G. S. Hwang et al., “Micro Thermoelectric Cooler: Multistage Planar,” *International Journal of Heat and Mass Transfer*, vol. 52, pp. 1843–1852, 2009.
3. B. L. Huang et. al, “Low-Temperature Characterization and Micro Patterning of Co-Evaporated Bi-Te and Sb-Te Films,” *Journal of Applied Physics,* in press, 2008.
4. A. Gross, G. Hwang, B. Huang, C. Lawrence, H. Kim, N. Ghafouri, S. W. Lee, K. Najafi, M. Kaviany, and C. Uher, “A Multistage In-Plane Micro Thermoelectric Cooler,” presented at the *MEMS 2008 Conference*.
5. L. W. da Silva and M. Kaviany, “Micro-TE Cooler: Interfacial Effects on Thermal and Electrical Transport,” *Int. J. Heat Transfer,* 47, pp. 2417–2435, 2004.
6. M. Kaviany, *Principles of Heat Transfer*, Wiley, NY, 2002.